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EXAMINER	
JOHNSON, BRIAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,886	SAHA, BRATIN	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-30 and 32-34* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 11-34 have been examined.

Acknowledgment of papers filed: remarks on 20 November 2007. The papers filed have been placed on record.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 11-13, 15-18, 20, 21, 23-27, 29, 30 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Lock Reservation (herein Koseki).

4. Regarding claim 11 Koseki discloses a machine-implemented method comprising: generating parallel processes in a data processing machine (page 130 Abstract); effecting synchronization between the parallel processes using processor speculation in the data processing machine (page 130 Abstract) to speculatively execute one or more instructions that read-modify- write a lock variable associated with a critical section and end speculation before performing the critical section (Page 132 Lock Reservation); and providing output resulting from the synchronized parallel processes.

5. Regarding claim 12 Koseki discloses the method of claim 11, wherein said generating parallel processes comprises running a software program that spawns multiple threads in the data processing machine (page 130 Abstract).

6. Regarding claim 13 Koseki discloses the method of claim 11, wherein said effecting synchronization comprises translating at least one high-level software instruction into at least one machine instruction that controls speculative execution in a processor (Page 130 footnote 1).

7. Regarding claim 15 Koseki discloses the method of claim 11, wherein said providing output comprises sending the output to another data processing machine (Page 135 Multiprocessor Considerations).

8. Regarding claim 16 Koseki discloses a article comprising a machine-readable storage medium embodying information indicative of instructions that when performed by one or more machines result in operations comprising: generating parallel processes in a data processing machine (Page 130 Abstract); effecting synchronization between the parallel processes using processor speculation in the data processing machine to speculatively execute one or more instructions that read-modify-write a lock variable associated with a critical section and end speculation before performing the critical

section (Page 132 Lock Reservation); and providing output resulting from the synchronized parallel processes.

9. Regarding claim 17 Koseki discloses the article of claim 16, wherein said generating parallel processes comprises running a software program that spawns multiple threads in the data processing machine (Page 130 Abstract).

10. Regarding claim 18 Koseki discloses the article of claim 16, wherein said effecting synchronization comprises translating at least one high-level software instruction into at least one machine instruction that controls speculative execution in a processor (Page 130 footnote 1)

11. Regarding claim 20 Koseki discloses the article of claim 16, wherein said providing output comprises sending the output to another data processing machine (Page 135 Multiprocessor Considerations).

12. Regarding claim 21 Koseki discloses a machine-implemented method comprising: speculatively executing machine instructions, including a memory access instruction, in a processing system to effect synchronization between parallel processes (Page 130 Abstract), wherein the speculatively executing comprises performing a speculative read- modify-write to a lock variable associated with a critical section; retiring the speculatively executed machine instructions to end speculation before

performing the critical section (Page 132 Lock Reservation); and maintaining cache coherence in the processing system during said executing and said retiring to identify a mis-speculation to effect the synchronization between the parallel processes (Page 138 Section 5.1).

13. Regarding claim 23 Koseki discloses the method of claim 21, wherein said speculatively executing machine instructions comprises speculatively executing machine instructions in the processing system comprising multiple processors (Page 135 Multiprocessor Considerations), and the mis-speculation comprises a memory dependency violation (Page 132 Lock Reservation).

14. Regarding claim 24 Koseki discloses the method of claim 21, wherein the mis-speculation comprises at least one of an interrupt, an external event, and a memory dependency violation (Page 132 Lock Reservation).

15. Regarding claim 25 Koseki discloses a system comprising: a processor having a processor architecture that provides speculative execution of machine instructions and exposes said speculative execution to program control through at least one machine instruction; and a memory coupled with the processor, the memory embodying information indicative of instructions (Page 130 Abstract), including the at least one machine instruction (Page 130 footnote 1), that result in synchronization between

parallel processes when performed by the processor with detection of mis-speculation; wherein performance of the instructions by the processor comprises performing a speculative read-modify-write to a lock variable associated with a critical section and ending speculation before performing the critical section (Page 132 Lock Reservation).

16. Regarding claim 26 Koseki discloses the system of claim 25, wherein the processor comprises a uniprocessor (Page 135 Multiprocessor Considerations).

17. Regarding claim 27 Koseki discloses the system of claim 25, wherein the processor comprises a multiprocessor (Page 135 Multiprocessor Considerations).

18. Regarding claim 29 Koseki discloses the system of claim 25, further comprising: a communication interface; and a virtual machine that translates the information, received via the communication interface, into the at least one machine instruction (Page 130 Footnote 1).

19. Regarding claim 30 Koseki discloses the system of claim 29, wherein the virtual machine comprises a Java virtual machine (Page 130 Footnote 1).

20. Regarding claim 34 Koseki discloses the processing system of claim 33, wherein said means for detecting a mis-speculation comprises means for maintaining cache coherence in the processing means (Page 138 Section 5.1).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koseki in view Transactional Memory (herein Moss).

23. Regarding claim 33, Koseki discloses a processing system comprising: processing means for speculatively executing machine instructions in response to a speculative execution instruction (Page 130 Abstract), including means for detecting a mis-speculation; means for treating multiple speculative instructions as a group for purposes of retirement such that the multiple speculative instructions are flushed from the processing means together and execution proceeds from an address in response to a detected mis-speculation to effect synchronization between parallel processes; wherein performance of the instructions by the processing means comprises performing a speculative read-modify-write to a lock variable associated with a critical section and ending speculation before performing the critical section (Page 132 Lock Reservation).

Koseki fails to disclose the use of a COMMIT instruction that retires multiple speculative instructions as a group.

Moss discloses such a COMMIT instruction (Page 290).

Koseki would have been motivated to use the COMMIT instruction to treat the multiple speculative instructions as a single instruction to simplify retirement of the instructions.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Koseki and include the COMMIT instruction of Moss.

24. Claims 14, 19, 22, 28 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koseki in view of Common Art.

25. Regarding claims 14 and 19 Koseki discloses the method of claim 11.

Koseki fails to disclose the remaining limitations.

Examiner takes Official Notice that an our-of-order processor with an out-of-order retirement unit is common in the art.

Koseki would have been motivated to utilize this technique to improve efficiency within the processing system.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Koseki and include the out-of-order processing

techniques found in common art. It is further obvious that, based on dependencies, some machine instructions would limit when other machine instructions are retired.

26. Regarding claim 22, Koseki discloses method of claim 21 including a system that maintains cache coherency.

Koseki fails to disclose that this system is based in invalidation.

Examiner takes Official Notice that this type of invalidation of cache systems is common in the art.

Koseki would have been motivated to utilize this technique because it is a common, simple, and efficient method of maintaining multiple levels of caches.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Koseki and include the cache invalidation system found in Common Art.

27. Regarding claim 28, Koski discloses the system of claim 27.

Koseki fails to disclose multiple processing units on a single die.

Examiner takes Official Notice that multiprocessing on a single die is common in the art.

Koseki would have been motivated to place the system on a single die for benefits in cost, efficiency, area, and power.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the multiprocessing system of Koseki and place it on a single die.

28. Regarding claim 32, Koseki discloses the system of claim 25.

Koseki fails to disclose an environmental sensor. further comprising an environmental sensor coupled with the processor.

Allowable Subject Matter

29. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art of record includes the limitations of claim 31 including operand indicating the starting location in case of a misspeculation. Since the misspeculation, in the case of Koseki, would be sent to a definite address, it would not be an obvious change to cause an instruction's operand to indicate such a starting address.

Response to Arguments

30. Applicant's arguments filed 20 November 2007 have been fully considered but they are not persuasive.

Applicant makes two arguments in favor of the patentability of the present application over the current art of record. Firstly, Applicant argues that Examiner's definition of "speculative" is improper. Secondly, Applicant argues that the speculative

nature of the system, even under Examiner's definition, does not end before the critical section, as required by the claim language.

Regarding the former, Examiner disagrees. Without further clarification on the word "speculative", it seems entirely proper to define it as a situation in which the processor acts without all required information, potentially requiring some work to be undone or discarded. Applicant, however, believes that the Specification of Koseki is inconsistent with Examiner's proposed definition, therefore, rendering Examiner's definition improper. Applicant quotes the following from Koseki page 4, paragraph 13:

The data processing machine may include an out-of-order processor/processing system that provides speculative execution of machine instructions, and this processor speculation capability is exposed to program control. Using processor speculation to implement synchronization among parallel processes may provide a significant advantage in that, if a critical section of a program happens to be uncontended at runtime (e.g., only one of the processes happens to need the critical section at a given time), then the overhead of traditional locking may be eliminated.

The citation above appears to be properly in line with Examiner's definition. Koseki's Specification describes speculative execution of machine instructions, a common technique in modern art. This technique involves executing program instructions without full knowledge of whether such definitions should be executed. If it is subsequently found that these instructions should not have been executed (perhaps by a mispredicted branch instruction), then the work completed on these instructions will be discarded. There is nothing in this citation inconsistent with Examiner's definition of "speculative".

Applicant, however, argues that Koseki's allegedly different definition and the claim language require use of "the speculative execution capabilities of modern processors." It appears that Applicant believes this phraseology carries with it a detectable and definable scope and bounds for the word "speculation". Examiner does not recognize such a definition. Consequently, the previous and current definition of speculation is used for the current rejection.

Regarding the latter argument, Applicant states that the speculation does not end prior to the beginning of the critical section. Applicant cites Koseki page 133 and 134. It is unclear what citation in these pages supports Applicant's alleged findings. Koseki's 3 steps of Lock Reservation on page 132 clearly indicate that the speculation occurs with respect to the acquisition of the lock. The critical section that the lock is protecting is not executed until the speculation is complete with respect to lock acquisition.

Examiner speculates that Applicant is mistaking the "critical lection" (the section of code requiring a lock for adequate thread synchronization) with the "unsafe regions" (portions of code involved in the the lock acquisition). In attempt to alleviate Applicant's concern with this matter, attention is directed to page 135, last partial paragraph of the first column, continuing onto the second column. This indicates that there is an embodiment in which these unsafe regions can be avoided and converted into safe regions.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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